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10/659,593	09/10/2003	Back-Woon Lee	YOM-0057	5378

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,593	LEE, BAEK-WOON	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-38* is/are pending in the application.

4a) Of the above claim(s) *4-6,19-32,34 and 35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-11,13-18,33 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *37 and 38* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5 April 2007 has been entered. Claims 1-11 and 13-38 are pending. Claims 4-6, 19-32, 34 and 35 have been previously withdrawn, and claim 12 has previously been cancelled. Claims 37-38 are currently withdrawn from consideration.

Response to Arguments

2. Applicant's arguments filed 3 April 2007 have been fully considered but they are not persuasive.

On page 10 of the applicant's remarks the applicant argues the claim rejections under 35 U.S.C. §103(a) as being unpatentable over Tsutomu and Yoshida et al. The applicant's argument is specifically against the Yoshida reference, where the applicant state that the Examiner improperly characterizes Figure 6 of Yoshida. The applicant states the Figure 6 of Yoshida shows drain electrode 42 of TFT 38 extending from the

data line 32 and a gate electrode 40 of TFT 38 extending from the gate line 36. The applicant then states that the drain electrode 42 would have a width substantially the same as the width of the data line 32 and likewise the gate electrode 40 has a width substantially the same as the width of the gate line 36. The applicant also states that Yoshida does not teach of white pixels. Further the applicant states that TFT 38 is formed at the intersection between gate line 36 and data line 32 and therefore each TFT 38 has projections 40 and 42 relied upon by the Examiner, as is well known in the prior art. The applicant concludes by stating: "Therefore, Yoshida does not teach or suggest that the white pixels are smaller than the other primary color as a result of a portion of the data line 32 or portion of the gate line 36 adjacent to the white pixels being wider than other portions of the respective data line 32 and/or gate line 36". The examiner respectfully disagrees.

First of all, the claim no longer requires that the white pixels are smaller than the other primary colors. Secondly, the examiner agrees with the applicant that the TFT 38 shown in Figure 6 of Yoshida contains the drain electrode 42 and the gate electrode 40, however, **the drain electrode is part of the data line and the gate electrode is part of the gate line**. This fact is well known in the art, and the examiner has cited Kim et al. (US 6,198,516) as proof of this, where Kim et al. specifically state in column 1, lines 45-52 that:

"A TFT 10 is formed at a portion of intersection of the gate line 1 and the data line 4. **The TFT 10 includes a gate electrode, i.e. a part of the gate line 1, a source electrode 7** and a drain electrode 8 disposed to be overlapped with the gate electrode.

The drain electrode 8 has a form withdrawn from the data line 4, and the source electrode 7 is disposed to be opposed with the drain electrode 8 and in contact with the pixel electrode 6."

Therefore, as stated previously by the examiner, **the drain electrode 42 is part of the data line 32** and the **gate electrode 40 is a part of the gate line 36**. Then, looking at Figure 6, it can be seen that the data lines extend in the north/south direction in the Figure, where the width of the data lines runs in the east/west direction in the Figure. Therefore, **the width of the data line where the drain electrode 42 extends is larger than the width of other parts of the line where a TFT is not to be formed**. The same is true for the gate lines. Looking at Figure 6, it can be seen that the gate lines extend in the east/west direction, where the width of the gate lines runs in the north/south direction. Therefore, **the width of the gate lines where the gate electrode 40 extends is larger than the width of other parts of the line where a TFT is not to be formed**. Hence, any display that has TFTs at the intersection of the pixels will have portions of the gate and data lines being larger than other portions, and when this well known idea is used with the display taught by Tsumoto, such that all of the pixels, i.e. red, green, blue and white, have a TFT at the intersection of gate and data lines, then the white pixels will have portions of the gate and data lines being larger than other portions of the lines.

The examiner fully understands the applicant's invention, and fully admits that Tsumoto and Yoshida et al. do not teach the applicant's **INVENTION**, however, the **CLAIMS** do NOT state that it can't be the portion of the line for forming the TFT that is

larger than the other portions, nor does the claim state that the larger portions are ONLY located on the gate and data lines next to the white pixels. What is required by the claim is that the display has gate lines, data lines, a switching element and red, green, blue and white pixels. Then the claim states merely that "a portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a line width larger than a width of other portions of the respective gate and data lines." This statement in the claim does not preclude the red, green and blue pixels from having a portion of their lines also having a larger width than other portions. Therefore, by using Yoshida et al. the examiner was merely showing that it is well known that in any device having gate lines and data lines which intersect and where a TFT is formed at the intersections, that the gate and data lines will have extensions therefrom and that this causes the data and gate lines to have a portion where the width is larger. If this is true for every pixel, when Yoshida is used with Tsumoto who teaches the red, blue, green and white pixels, then the white pixels will end up with portions of the gate and data lines being larger than other portions of the lines. Therefore, with respect to the argument presented by the applicant on page 12, lines 3-12, Tsumoto and Yoshida et al. do teach that the gate lines and data lines adjacent to the white pixels will have a portion larger than other portions of the lines, and thus the combination does teach all elements of the invention.

Election/Restrictions

3. Newly submitted claims 37-38 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The previously presented claims are drawn to an invention required that the line width of a portion of the data or gate lines to be larger than another portion of the lines, whereas claims 37 and 38 require that the black matrix enclosing the white pixel is wider than other portions of the black matrix.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 37-38 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-3, 7-11 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutomu (JP 2001-296523) in view of Yoshida et al. (US 6,542,212).

Regarding claim 1, Tsutomu discloses a display device comprising:

a plurality of pixels including color pixels and a white pixel (Fig. 1);

a plurality of gate lines extending in a first direction for transmitting a gate signal to the pixels (Fig. 7 shows the gate lines extending in a row direction); and

a plurality of data lines extending in a second direction for transmitting data signals to the pixels (Fig. 7 shows the data lines extending in a column direction).

Tsutomu fails to explicitly teach each pixel including a pixel electrode and a switching element, and wherein a portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a line width larger than a width of other portions of the respective gate and data lines.

Yoshida et al. discloses of a device where

each pixel includes a pixel electrode and a switching element (Figure 6 and column 8, lines 25-45 explain that a TFT 38 is formed, which is a switching element,

where the pixel electrode would be formed in the intersection area of the gate and data lines shown, which is well known in the art.), and

wherein a portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a line width larger than a width of other portions of the respective gate and data lines (Figure 6 shows that the projections from the data lines 32 shown as 42 are larger than the width of the rest of the data lines, and also the width of gate lines 36 are larger at portion 40 than at the other portions of the gate lines. While the projections 42 and 40 form the source and gate electrodes for the TFT, respectively, there are a projections of the data and gate lines and therefore cause the width of the data and gate lines to be larger at these portions.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Yoshida et al. in the display of Tsutomu such that each pixel in the display, including the white pixels will have a portion of the data and gate lines larger than other portions of the lines in order to provide a well-known method of activating the pixel when it is being addressed.

Regarding claim 2, Tsutomu and Yoshida et al. disclose the display device of claim 1.

Tsutomu also discloses wherein the three primary color pixels include red, green and blue pixels (Fig. 1).

Regarding claim 3, Tsutomu and Yoshida et al. disclose the display device of claim 2.

Tsutomu also discloses a display wherein the green pixel is spaced apart from the white pixel (Fig. 1).

Regarding claim 7, Tsutomu and Yoshida et al. disclose the display device of claim 1.

Tsutomu also discloses a display wherein the pixels are arranged in sequence along the first direction (Fig. 1).

Regarding claim 8, Tsutomu and Yoshida et al. disclose the display device of claim 7.

Tsutomu also discloses a display wherein the color pixels include red, green and blue pixels and the red pixel, the green pixel, the blue pixel, and the white pixel are arranged in sequence (Fig. 1).

Regarding claim 9, Tsutomu and Yoshida et al. disclose the display device of claim 1.

Tsutomu also discloses a display wherein the color pixels have substantially equal size (Fig. 1).

Regarding claim 10, this claim is rejected under the same rationale as claim 1.

Regarding claim 11, Tsutomu and Yoshida et al. disclose the display device of claim 10.

Yoshida et al. also discloses wherein the gate lines intersect the data lines (Figure 6) and the at least one portion having the larger line width does not directly intersect other larger line width portions of the respective gate and data lines (Figure 6 shows that the portion 42 of data line 32 that is larger does not directly intersect any other of the larger portions of the data lines, as well as the portion 40 of the gate line 36 that is larger does not directly intersect any other of the larger portions of the gate lines.).

Regarding claim 36, Tsutomu and Yoshida et al. disclose the display device of claim 1.

Tsutomu also discloses wherein the white pixel is smaller than the three primary color pixels (Fig. 1).

7. Claims 13 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka (US 5,929,843) in view of Yoshida et al. (US 6,542,212).

Regarding claims 13 and 33, Tanioka discloses a device and method of driving a display device (see abstract 1-7) comprising:

a plurality of dots (Fig. 2, where 51 is a dot), each dot including red, green, blue, and white pixels (Fig. 2),

a plurality of gate lines for transmitting gate signals to the pixels (Fig. 7, driver 49 drives the gate lines), and

a plurality of data lines for transmitting data signals to the pixels (Fig. 7, driver 47 drives the data lines), the device comprising:

a gate driver (Fig. 7, driver 49) supplying the gate signals to the gate lines;

a data driver (Fig. 7, driver 47) supplying the data voltages to the data lines; and

an image signal modifier (Fig. 1) for converting three-color image signals into four-color image signals (Fig. 1 shows a 3-color signal being converted into a 4-color signal at lines 8), optimizing the four-color image signals (the pseudo-halftone processor 14-1 to 14-3 optimizes the 4-color signal), and supplying the optimized image signals to the data driver such that the data driver converts the optimized image signals to the data voltages (Fig. 1, where R", G", B", and W" are the optimized signals and as seen in Fig. 7, these signals are supplied to the display device and the data driver).

Tanioka fails to explicitly teach where a portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a line width larger than a width of other portions of the respective gate and data lines.

Yoshida et al. discloses of a liquid crystal display where a portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a line width larger than a width of other portions of the respective gate and data lines (Figure 6 shows that the projections from the data lines 32 shown as 42 are larger than the width

of the rest of the data lines, and also the width of gate lines 36 are larger at portion 40 than at the other portions of the gate lines. While the projections 42 and 40 form the source and gate electrodes for the TFT, respectively, there are a projections of the data and gate lines and therefore cause the width of the data and gate lines to be larger at these portions.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Yoshida et al. in the display of Tanioka such that each pixel in the display, including the white pixels will have a portion of the data and gate lines larger than other portions of the lines in order to provide a well-known method of activating the pixel when it is being addressed.

8. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka (US 5,929,843) in view of Yoshida et al. (US 6,542,212) and further in view of Morita (US 2002/0196243).

Regarding claim 14, Tanioka and Yoshida et al. disclose the device of claim 13.

Tanioka also discloses a device wherein the image signal modifier comprises:

a data converter converting three-color image signals into four-color image signals (Fig. 1, the section comprising 13-1, 13-2, 13-3, and 11 is a data converter);

a data optimizer optimizing the four-color image signals from the data converter (14-1 to 14-4 is the data optimizer); and

a data output unit supplying the optimized image signals to the data driver (Fig. 7, display controller 44 performs this function).

Tanioka and Yoshida et al. fail to teach supplying the image signals to the data driver in synchronization with a clock; and a clock generator generating the clock, the data driver operating in synchronization with the clock.

Morita discloses a liquid crystal display where supplying the image signals to the data driver is in synchronization with a clock (see para. 239); and a clock generator generating the clock (see para. 239, where there is a control signal generation circuit 74 providing the clock), the data driver operating in synchronization with the clock (para. 239).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Morita in the device of Tanioka and Yoshida et al. in order to have a device where the data driver received image signal at the same rate it output data signals to the display.

Regarding claim 18, Tanioka, Yoshida et al. and Morita disclose the device of claim 14.

Tanioka also discloses wherein the data output unit outputs the optimized image signals by group of four optimized image signals (Figure 7 and column 4, lines 63-65 explain that the display controller 44 reads out the RGB and W binary data from the frame memory and supplies them to a shift register in a serial manner.).

Allowable Subject Matter

9. Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Relative to dependent claim 15, the major difference between the prior art of record (Tsutomu, Tanioka) and the instant invention, is that the prior art does not teach optimized image signals determined by: W'=Min(W.sub.0, 255); R'=R.sub.0+Max(0, W.sub.0-255); G'=G.sub.0+Max(0, W.sub.0-255); and B'=B.sub.0+Max(0, W.sub.0-255).

Regarding dependent claim 16, the major difference between the prior art of record (Tsutomu, Tanioka) and the instant invention, is that the prior art does not teach optimized image signals determined by: G'=G.sub.0+(255-Max(R.sub.0, G.sub.0, B.sub.0)); and B'=B.sub.0+(255-Max(R.sub.0, G.sub.0, B.sub.0)), (**Note the claim objection above regarding this claim. The preceding analysis using "B'" and "B.sub.0" was how the claim was best understood to be intended by the applicant).

Relative to dependent claim 17, the major difference between the prior art of record (Tsutomu, Tanioka) and the instant invention, is that the prior art does not teach optimized image signals determined by: W'=(W.sub.0+Average(R.sub.0, G.sub.0, B.sub.0))/2; R'=R.sub.0+(W.sub.0-Average(R.sub.0, G.sub.0, B.sub.0))/2;

G'=G.sub.0+(W.sub.0-Average(R.sub:0, G.sub.0, B.sub.0))/2; and

B'=B.sub.0+(W.sub.0-Average(R.sub.0, G.sub.0, B.sub.0))/2.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zhong et al. (US 5,994,721) disclose of a display device with red, green, blue and white pixels.

Kim et al. (US 6,198,516) disclose that the gate electrode is a part of the gate line and that the drain electrode is a part of the data line.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

20 April 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER